IN THE CLAIMS

Please cancel claim 13 without prejudice.

Please amend claims 1, 4, 5, and 9.

1. (Currently Amended) A method for fabricating a [capacitor formed on a substrate wherein said capacitor is utilized in a] semiconductor device[, said method] comprising the steps of:

designating a salicide gate for use with said semiconductor device;

configuring a self-aligned contact for use with said semiconductor device; ~~and~~

patterning a poly gate on said substrate with a hard mask;

performing a cell implant thereof;

depositing sequentially TEOS, SiN, BPTEOS on said substrate;

performing an IPO-1 planarization upon a layer formed on said substrate; and

combining said salicide gate and [a] said self-aligned contact in a memory cell area of said semiconductor device to thereby permit the efficient shrinkage of memory cell size without an additional mask or weakening of associated circuit performance.

2. - 3. (cancelled)

4. (Currently Amended) A method for fabricating a [capacitor formed on a substrate wherein said capacitor is utilized in a] semiconductor device[, said method] comprising the steps of:

designating a salicide gate for use with said semiconductor device;

configuring a self-aligned contact for use with said semiconductor device;

patterning a poly gate on said substrate with a hard mask;

performing a cell implant thereof;

depositing sequentially TEOS, SiN, BPTEOS on said substrate;

performing an IPO-1 planarization upon a layer formed on said substrate;

combining said salicide gate and [a] said self-aligned contact in a memory cell area of said semiconductor device to thereby permit the efficient shrinkage of memory cell size without an additional mask or weakening of associated circuit performance; and

performing an anisotropic etch back thereof to stop on said poly gate utilizing high selectivity between said poly gate and said anisotropic etch back, wherein said anisotropic etch back comprises anisotropic etch back based on a combination of oxide and SiN.

5. (Currently Amended) A method for fabricating a [capacitor formed on a substrate wherein said capacitor is utilized in a] semiconductor device[, said method] comprising the steps of:

designating a salicide gate for use with said semiconductor device;

configuring a self-aligned contact for use with said semiconductor device;

patterning a poly gate on said substrate with a hard mask;

performing a cell implant thereof;

depositing sequentially TEOS, SiN, BPTEOS on said substrate;

performing an IPO-1 planarization upon a layer formed on said substrate; [a] and

combining said salicide gate and [a] said self-aligned contact in a memory cell area of said semiconductor device to thereby permit the efficient shrinkage of memory cell size without an additional mask or weakening of associated circuit performance;

defining a logic poly gate;

performing an LDD implant upon said substrate; and

forming a spacer deposition layer upon said substrate.

6. (Original) The method of claim 5 further comprising the steps of:

performing a spacer TEOS dry etch followed by a stop at SiN;

utilizing an additional photo mask to open an associated DRAM array; and

utilizing a wet dip upon said substrate and said layers thereof to remove a spacer TEOS.

7. (Original) The method of claim 6 further comprising the steps of:

performing a spacer SiN dry etch upon said substrate and said layers thereof followed by a stop on a TEOS; and

utilizing a wet dip upon said substrate and said layers thereof to remove said spacer TEOS.

8. (Original) The method of claim 7 further comprising the step of:

forming a Co-salicide upon said substrate for use with said semiconductor device.

9. (Currently Amended) A method for fabricating [a capacitor formed on a substrate wherein said capacitor is utilized in a] semiconductor device[, said method] comprising the steps of:

designating a salicide gate for use with said semiconductor device;

configuring a self-aligned contact for use with said semiconductor device;

patterning a poly gate on said substrate with a hard mask;

performing a cell implant thereof;

depositing sequentially TEOS, SiN, BPTEOS on said substrate;

performing an IPO-1 planarization upon a layer formed on said substrate; a

combining said salicide gate and [a] said self-aligned contact in a memory cell area of said semiconductor device to thereby permit the efficient shrinkage of memory cell size without an additional mask or weakening of associated circuit performance;

performing an anisotropic etch back thereof to stop on said poly gate utilizing high selectivity between said poly gate and said anisotropic etch back, wherein said anisotropic etch back comprises anisotropic etch back based on a combination of oxide and SiN;

defining a logic poly gate;

performing an LDD implant upon said substrate;

forming a spacer deposition layer upon said substrate;

performing a spacer TEOS dry etch followed by a stop at SiN;

utilizing an additional photo mask to open an associated DRAM array;

utilizing a wet dip upon said substrate and said layers thereof to remove a spacer TEOS;

performing a spacer SiN dry etch upon said substrate and said layers thereof followed by a stop on a TEOS;

utilizing a wet dip upon said substrate and said layers thereof to remove said spacer TEOS;

forming a Co-salicide upon said substrate for use with said semiconductor device; and

utilizing said capacitor formed between a metal-one layer and a metal-two layer upon said substrate in said semiconductor device, wherein said capacitor comprises an MIM capacitor.

10. (Previously Presented) The method of claim 9 wherein said semiconductor device comprises a DRAM-based semiconductor device.

11. (Previously Presented) The method of claim 9 wherein said poly gate comprises a DRAM poly gate.

12. (Previously Presented) The method of claim 9 wherein said cell implant comprises a cell LDD implant.

13. – 29. (Cancelled)